REMARKS

Claims 1-9, 11-19, 21-27, 29, and 31-37 are pending in this application. By this Response, claims 1-3, 5, 7-9, 11-13, 15, 17-19, 21-23, 25, 27, 29, and 31-33 are amended, claims 10, 20, 28, and 30 are canceled, and claims 34-37 are added. Claims 31-33 are amended to recite a control processor and a plurality of controlled processors, at least one processor of the plurality of controlled processors being selected to operate in a shared operational state, the at least one processor being at least one first controlled processor, and one processor from the plurality of controlled processors being selected to operate in an isolated operational state, the one processor being a second controlled processor. Support for these features may be found at least in Figures 47 and 58 and the corresponding descriptions of the present specification. Claims 1-3, 5, 7-9, 11-13, 15, 17-19, 21-23, 25, 27, 29, and 31-33 are amended for clarification purposes to recite "controlled" processors and, in appropriate claims, to expand acryonyms. Claims 34-37 are added to recite additional features of the present invention. Support for the addition of claims 34-37 may be found at least in Figures 57-58 and the corresponding descriptions of the present specification. No new matter has been added by any of the above amendments or addition of claims. Reconsideration of the claims is respectfully requested in view of the following remarks.

I. Telephone Interview

Applicants thank Examiner Parthasarathy for the courtesies extended to Applicants' representative during the June 29, 2007 telephone interview. During the telephone interview, the above amendments and the distinctions of the claims over the cited art were discussed. Examiner Parthasarathy agreed that the above amendments to the claims overcome the objections and rejections set forth in the Office Action with regard to 35 U.S.C. § 112 and 101. Examiner Parthasarathy stated that she believed that the amendments overcome the rejections based on the Sibert reference but would need to look at the reference in more detail once a formal response was filed before making a final determination. Moreover, Examiner Parthasarathy requested that the claims be

amended for clarification to recite that the "first" and "second" processors are "controlled" processors. Finally, Examiner Parthasarathy requested that the title of the invention be amended to be more descriptive of the claimed invention. The substance of the telephone interview is summarized in the following remarks.

II. Claim Objections

The Office Action objects to claims 1, 8, 18, 28, and 31 because of a number of informalities. By this Response, these claims are amended where appropriate to correct these informalities. Specifically, claim 1 is amended to recite an "encryption request" as suggested by the Examiner, claims 8 and 18 are amended to expand the acronym "DMA", and claim 31 is amended to recite "a shared memory."

With regard to the Examiner's assertion that claim 1 should be amended to recite "sending an encryption request from the first processor to the second processor" rather than "sending an encryption request from a first processor in the at least one first processor to the second processor," Applicants respectfully disagree. Claim 31 from which claim 1 depends recites "at least one first controlled processor." There may be a plurality of first controlled processors, e.g., there may be 7 SPUs in an exemplary embodiment that operate in a shared mode while 1 SPU operates in an isolated mode (see, for example, Figure 57 of the present specification). Therefore, claim 1 is reciting that one of these first controlled processors is sending an encryption request to the second controlled processor. Thus, the language of claim 1 is correct as it currently stands.

Regarding the Examiner's assertion that claim 31 should be amended to recite "the second processor," clarifying amendments are made by this Response to correct the recitation of "first" controlled processor and "second" controlled processor in claims 31-33. Thus, Applicants respectfully submit that amended claims 31-33 correctly recite the subject matter Applicants' regard as their invention.

In view of the above, Applicants respectfully request withdrawal of the objection to claims 1, 8, 18, and 31.

III. Rejection under 35 U.S.C. § 101

The Office Action rejects claims 1-33 as being allegedly directed to non-statutory subject matter because independent claims 31-33 are allegedly not limited to tangible embodiments. During the June 29, 2007 telephone interview, Examiner Parthasarathy agreed that the rejection under 35 U.S.C. § 101 was overcome by the above amendments to the claims. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 1-33 under 35 U.S.C. § 101.

IV. Rejection under 35 U.S.C. § 112, Second Paragraph

The Office Action rejects claims 1-33 under 35 U.S.C. § 112, second paragraph as allegedly being indefinite. With regard to claims 31-33, by this Response claims 31-33 are amended to correct the recitation of "first controlled processor" and "second controlled processor" in the claims. Thus, Applicants respectfully submit that claims 31-33 are not indefinite.

Regarding claims 10, 20, and 30, these claims are canceled by this Response and thus, the rejection of these claims is rendered moot. In view of the above, Applicants respectfully submit that claims 1-33 are not indefinite. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 1-33 under 35 U.S.C. § 112, second paragraph.

V. Rejection under 35 U.S.C. § 102(e)

The Office Action rejects claims 1-33 under 35 U.S.C. § 102(e) as allegedly being anticipated by Sibert (U.S. Patent No. 7,124,170). This rejection is respectfully traversed.

Claim 31, which is representative of the other rejected independent claims 32 and 33 with regard to similarly recited subject matter, reads as follows:

31. A method, in a multiprocessor system, the multiprocessor system comprising a control processor and a plurality of controlled processors, the method comprising:

selecting at least one controlled processor of the plurality of controlled processors to operate in a shared operational state;

selecting a second controlled processor from the plurality of controlled processors to operate in an isolated operational state;

configuring the at least one first controlled processor of the multiprocessor system to be in the shared operational state, wherein the shared operational state causes the at least one first controlled processor to operate using a common memory accessible by the plurality of controlled processors in the multiprocessor system;

configuring the second controlled processor of the multiprocessor system, via loading and executing initialization code in the second controlled processor, to be in the isolated operational state, wherein the isolated operational state causes a local memory associated with the second controlled processor to be not accessible by the at least one first controlled processor;

executing first code within the second controlled processor in a secure manner by virtue of the isolated operational state; and

executing second code within the at least one first controlled processor in an unsecured manner by virtue of the shared operational state. (emphasis added)

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). Applicants respectfully submit that Sibert does not identically show every element of the claimed invention arranged as they are in the claims. Specifically, Sibert does not teach those features of claim 31 emphasized above or the similar features found in independent claims 32 and 33.

Sibert is directed to a secure processing unit (SPU) which can perform both security functions and other information appliance functions using the same set of

hardware resources. The SPU of Sibert is provided in a tamper resistant package that has a plurality of sensors for detecting various types of tampering, e.g., a breach sensor, a light sensor, a radiation sensor, a temperature sensor, and input error sensor, etc (see Figure 1A). The SPU has an external bus through which it may communicate with external peripheral devices. The communication is preferably outbound only, but may support inbound communication such that external devices may access an internal memory of the SPU. In such a case, processor security registers may be used to indicate which internal resources permit or do not permit external access (column 6, lines 42-56).

The SPU, via software running on the SPU, may be used to perform digital rights management that governs encryption/decryption of, access to, payment for, and/or reporting of digital music content being played, etc. (column 6, lines 62-66). Memory protection within the SPU may be performed in a number of different ways including the memory management unit isolating memory regions accessible to different software modules. Certain regions of an internal memory of the SPU may be designated as critical and access to those regions restricted to certain processor operating modes (column 8, lines 47-50). At least one cryptographic key may be stored internally in the SPU for use in encryption/decryption (column 16, lines 1-6).

Nowhere in Sibert is there any teaching, or even suggestion, to select at least one controlled processor of a plurality of controlled processors to operate in a shared operational state and select one controlled processor from the plurality of controlled processors to operate in an isolated operational state. In Sibert, the SPU is intended to be the only processor in the system with the SPU performing security functions and other functions that would otherwise be performed by a general purpose processor. But, it is implied that it is possible that the SPU could be used in conjunction with a single general purpose processor (see column 5, lines 44-62). However, even in the case of the SPU being used with a general purpose processor, there is no selection operation performed to determine whether the SPU or the general purpose processor will be placed in a shared operational mode or an isolated operational mode. To the contrary, the SPU will always perform the encryption/decryption operations, and thus operate in a secure mode, by virtue of its internal mechanisms which are not present in the general purpose processor. Thus, there is no selection performed in Sibert and there is no motivation to perform such

a selection in Sibert because there really are no other options available from which to select.

Thus, in view of the above, Applicants respectfully submit that Sibert does not teach each and every feature of independent claim 31 as is required under 35 U.S.C. § 102(e). Furthermore, for similar reasons, Sibert does not teach each and every feature of independent claims 32-33. At least by virtue of their dependency on claims 31-33, Sibert does not teach each and every feature of dependent claims 1-9, 11-19, 21-27, and 29. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 1-9, 11-19, 21-27, 29, and 31-33 under 35 U.S.C. § 102(e).

In addition to the above, Sibert does not teach the specific features recited in dependent claims 1-9, 11-19, 21-27, and 29. For example, with regard to claims 3, 13, and 23, Sibert does not teach the feature of writing a request to a mailbox corresponding to the second controlled processor and the second controlled processor checking the mailbox. The Office Action alleges that this feature is taught by Sibert in that Sibert, as described in column 17, lines 23-48, provides security registers that indicate whether they have been tampered with or not. The security registers of Sibert provide one bit for each region of an internal memory and are used to indicate, for example, whether the memory region is critical or not, whether it is to be cleared in response to detected tampering, etc. The security registers of Sibert do not provide a mailbox function in which requests for encryption operations are written to the mailbox. Thus, despite the Office Action's allegations, Sibert does not in fact teach the features of a mailbox as recited in claims 3, 13, and 23.

As a further example, Sibert does not teach the features of reading initialization software code from a common memory to be executed on the controlled processor to be placed in an isolated mode of operation and authenticating the initialization software code, as recited in claims 5, 15, and 25. The Office Action alleges that Sibert teaches these features at column 15, line 66 to column 16, line 25 and column 17, lines 23-48. Column 15, line 66 to column 16, line 25 merely teach that monitor software may be established within the SPU along with a secret cryptographic key. In fact, column 16, lines 21-25 describe the initialization process as being to fix the software physically in secure read-only memory of the SPU as part of the manufacturing process. Thus, there is

no need to read the monitor software from a common memory since it is already fixed in the SPU. Moreover, there would be no reason to authenticate the monitor software since it was fixed at the time of manufacture in a memory that is not modifiable.

Column 17, lines 23-48 merely describes that the internal memory is divided into regions, each of which has a security register bit that indicates whether the region is to be cleared when tampering is detected. This section further teaches that a backup process may periodically run that obtains a public backup key and combines SPU identity information with the result being encrypted and stored. Nowhere in this section is there any teaching of reading initialization software code from a common memory to be executed on a controlled processor to be placed in an isolated mode of operation and authenticating the initialization software code.

As yet another example, Sibert does not teach identifying an encryption process and an encryption algorithm from a plurality of encryption processes and encryption algorithms based upon an encryption request and loading encryption software code corresponding to the identified encryption process and encryption algorithm by reading it from a common memory into the isolated mode processor's local memory, as recited in claims 9, 19, and 29. The Office Action alleges that these features are taught by Sibert at column 17, lines 23-48 and column 20, lines 19-67. The teachings of column 17, lines 23-48 have been addressed above and shown to only teach (1) the internal memory is divided into regions, each of which has a security register bit that indicates whether the region is to be cleared when tampering is detected; and (2) a backup process may periodically run that obtains a public backup key and combines SPU identity information with the result being encrypted and stored. There is nothing in column 17 that even remotely resembles the features of claims 9, 19, and 29.

Furthermore, column 20, lines 19-67 merely teaches that the SPU holds a secret key in internal memory, this secret key may be generated inside the SPU, and that the SPU may store different keys for different purposes. This section also teaches that the SPU may generate a plurality of secret keys as required. Moreover, this section discusses that the SPU has a publicly available device ID value which may be stored internally or externally under protection of a secret key. The SPU may further have at least one asymmetric key pair, a cryptographic certificate, and one or more validation keys. While

this section discusses a number of keys, there is no teaching or suggestion regarding identifying an encryption process and an encryption algorithm from a plurality of encryption processes and encryption algorithms based upon an encryption request and loading encryption software code corresponding to the identified encryption process and encryption algorithm by reading it from a common memory into the isolated mode processor's local memory. Thus, despite the allegations made by the Office Action, Sibert in fact does not teach the features of claims 9, 19, and 29.

The other dependent claims not specifically addressed above also contain features which, when taken alone or in combination with the features from which they depend, are not taught by the Sibert reference. Accordingly, Applicants respectfully request withdrawal of the rejection of claims 1-9, 11-19, 21-27, and 29.

VI. Newly Added Claims 34-37

Claims 34-37 are added to recite additional features of the present invention. Applicants respectfully submit that the Sibert reference does not teach any of the features recited in claims 34-37. Accordingly, Applicants respectfully request prompt and favorable consideration of claims 34-37.

VII. Conclusion

It is respectfully urged that the subject application is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

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